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Real-Time Chessboard Digitization: A Vision-Based System for Low-Cost Embedded Platforms

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Abstract: The integration of computer vision into real-world applications is often hindered by the high computational demands of deep learning models and the associated cost of hardware. This paper presents a novel, comprehensive solution for the real-time digitization of a physical chessboard, specifically designed for low-cost embedded platforms. We introduce a complete system that combines efficient classical computer vision algorithms for chessboard localization with a custom-designed, lightweight Convolutional Neural Network (CNN) for piece recognition. The core of our innovation lies in the use of a low-cost, open-source RISC-V platform, which is augmented with a custom, tightly coupled hardware accelerator to offload the most computationally intensive tasks. Our system demonstrates a chessboard localization accuracy of 99.5% and a piece recognition accuracy of 98.2%. Critically, it achieves an average processing latency of 150 milliseconds per frame, enabling true real-time operation on hardware that is an order of magnitude more affordable and power-efficient than conventional GPU-based systems. This work validates a crucial hardware-software co-design paradigm for deploying complex AI tasks on resource-constrained devices, paving the way for a new generation of affordable, intelligent edge applications.

Keywords: Computer Vision, Chessboard, Deep Learning, Embedded Systems, RISC-V, Hardware Acceleration, Real-time.

INTRODUCTION

The proliferation of deep learning and computer vision has ushered in a new era of intelligent systems capable of perceiving and interacting with the physical world [8, 29]. From autonomous vehicles to medical imaging, these technologies are transforming industries and creating novel applications [1, 24]. One such domain where computer vision holds significant promise is in the automation and analysis of classic board games, particularly chess. Automating the real-time digitization of a physical chessboard offers numerous benefits, including enabling human-robot interaction [16, 17, 18], enhancing training and analysis through digital archives, and creating accessible tools for players with disabilities.

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Existing solutions for chessboard digitization typically fall into two categories: high-end systems utilizing powerful graphics processing units (GPUs) and computationally complex algorithms, or purpose-built, often expensive, hardware [19]. Many of these approaches rely on complex robotics [16], powerful desktop computers, or cloud-based processing, making them inaccessible for widespread, low-cost applications. While previous work has explored the use of neural networks for recognizing chess pieces [9, 10, 27], and others have focused on chessboard detection [23], a significant research gap remains in integrating these components into a single, cohesive, and most importantly, affordable system that operates in real-time on a low-power, embedded platform.

The primary challenge lies in the trade-off between computational complexity and real-time performance on resource-constrained hardware. Deep neural networks, while highly effective for image classification, often require substantial memory and processing power [4, 7, 29]. Deploying such models on embedded systems, which are constrained by size, power consumption, and cost, necessitates a paradigm shift in both algorithm design and hardware-software co-development [14, 20, 21, 22].

This paper presents a novel, cost-effective, vision-based system for the real-time digitization of a physical chessboard. We propose a full-stack solution that combines computationally efficient computer vision techniques for chessboard localization with a highly optimized, lightweight convolutional neural network (CNN) for piece recognition. The entire system is designed and implemented on a low-cost, open-source hardware platform, demonstrating the feasibility of deploying complex AI tasks on edge devices. Our contributions are threefold: (1) a robust and efficient pipeline for real-time chessboard and piece detection, (2) the development and optimization of a tailored CNN model that achieves high accuracy with a minimal memory footprint, and (3) a comprehensive system integration on a low-cost embedded platform, providing a practical blueprint for affordable vision-based systems.

2. METHODS

2.1 System Architecture

The proposed system follows a modular, three-stage processing pipeline: image acquisition, chessboard localization, and piece recognition and digitization. A monocular camera captures a top-down view of the chessboard. The captured image is then processed in real-time on the embedded platform. The first stage, chessboard localization, uses classical computer vision algorithms to identify the corners and grid lines of the board. Once the board is located, the image is warped to a standardized perspective, and each of the 64 squares is isolated. The second stage, piece recognition, involves feeding these individual square images to a lightweight CNN classifier to determine the state of each square (empty or occupied by a specific piece). Finally, the results from all squares are aggregated to generate a complete digital representation of the board in a standardized format, such as Forsyth-Edwards Notation (FEN) [28].

2.2 Hardware Platform

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To ensure affordability and low power consumption, the system is built upon a low-cost, open-source embedded platform featuring a RISC-V processor [12, 13, 14]. This choice is strategic, as RISC-V offers a flexible and extensible instruction set architecture (ISA) that allows for hardware-software co-design and the integration of specialized accelerators [15, 36, 37]. The specific platform utilizes a RISC-V core with a tightly coupled hardware accelerator for performing the matrix multiplications essential for CNN inference [38]. This approach significantly reduces the computational load on the main processor, enabling real-time performance that would be unattainable with a purely software-based solution on similar hardware [39]. The camera sensor is a low-cost module capable of capturing a video stream at a resolution suitable for the task. The entire setup is designed to be powered by a small battery or a low-voltage power supply.

2.3 Chessboard Localization

The localization of the chessboard is a critical first step. We adopted a robust, two-phase approach to handle varying lighting conditions and minor camera misalignments. The first phase uses a combination of grayscale conversion and Gaussian blurring to reduce noise, followed by the Canny edge detection algorithm to identify prominent edges in the image [41]. The Canny algorithm is a multi-stage process,

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beginning with noise reduction to smooth the image and remove unwanted artifacts, followed by the computation of intensity gradients to highlight potential edges. Non-maximum suppression is then applied to thin the edges and retain only the most prominent ones, culminating in hysteresis thresholding to connect the final edge segments. This method is computationally efficient and effective at highlighting the strong, linear features of the chessboard.

In the second phase, we apply the probabilistic Hough transform to detect straight lines from the Canny edge map [42]. The Hough transform works by mapping points in the image space to parameter space, where a line is represented as a single point. This makes it highly robust to noise and missing edge segments. The parameters of the Hough transform were carefully tuned to specifically identify a dense set of horizontal and vertical lines, which correspond to the grid of the chessboard. Once a candidate set of lines is identified, the intersections of these detected lines are then computed [35]. This geometric analysis is crucial. We filter out spurious intersections and identify the set of 81 intersection points that form a regular 8x8 grid. By analyzing the spatial relationships and geometric properties of these intersection points, we can identify the four corners of the chessboard and the complete 8x8 grid. This grid information allows for a perspective transformation that rectifies the image of the board, making each square a perfectly aligned region for subsequent analysis. This method avoids the need for complex, marker-based calibration [23] and is computationally lightweight, suitable for the embedded platform.

2.4 Chess Piece Recognition

Piece recognition is the most computationally intensive part of the pipeline. To address the constraints of our hardware, we designed a custom, lightweight CNN model. This model is inspired by highly efficient architectures such as MobileNetV2 [5] and SqueezeNet [33], which use depthwise separable convolutions and efficient bottleneck layers to achieve high accuracy with a dramatically reduced number of parameters and computational operations [6, 29]. Our model, dubbed ChessNet, has a minimal number of layers and channels, specifically tailored for the classification task of 13 classes: 12 unique chess pieces (Pawn, Knight, Bishop, Rook, Queen, King, in both black and white) and an empty square.

The training dataset was a mix of real-world images and a large number of synthetically generated images [10]. This data augmentation strategy proved crucial for creating a robust model that can handle variations in lighting, background, and piece orientation. Each of the 64 localized square images is fed to the pre-trained ChessNet model, which outputs a probability distribution over the 13 classes. The square is assigned the class with the highest probability. The synthetic data was generated using a 3D rendering engine, which allowed us to create a vast number of unique images by programmatically controlling variables such as camera angle, lighting direction, shadow intensity, and surface texture. This approach provides a nearly infinite source of training data, significantly reducing the risk of overfitting and improving the model's generalization capabilities on unseen, real-world chess sets.

2.5 Chess State Digitization

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The final stage of the pipeline integrates the output of the chessboard localization and piece recognition modules. For each of the 64 squares, the system retrieves the recognized piece (or 'empty' label) and its location on the 8x8 grid. This data is then used to construct the FEN string, a standard text-based representation of the board state [28]. The FEN string is a powerful and compact way to describe the current state of a chess game in a single line of text. It includes information on piece placement, whose turn it is to move, castling rights, and the potential for en passant captures. The FEN string is continuously updated in real-time, providing a seamless digital output of the physical game state. The system also includes a simple move validation layer, comparing the current FEN to the previous one to detect single-move changes. This is done by comparing the FEN strings and identifying the squares from which pieces have moved. This logic allows the system to not only report the board state but also to identify and record the moves of the game.

2.6 In-Depth Analysis of Hardware-Software Co-Design and Acceleration

The primary objective of this research is to demonstrate the feasibility of real-time chessboard digitization on an affordable, low-cost embedded platform. While the algorithmic choices—such as the lightweight ChessNet CNN and efficient classical computer vision techniques—are crucial, they are not sufficient on their own to overcome the significant computational and energy constraints of this class of hardware. A purely software-based approach, where the entire deep learning inference is executed on a general-purpose processor, would result in prohibitively high latency and power consumption, rendering the system non-real-time and impractical for extended use [20, 21]. To surmount this challenge, we adopted a holistic hardware-software co-design methodology, strategically offloading the most computationally intensive tasks to a custom hardware accelerator tightly integrated with the main processor.

The open-source nature of the RISC-V Instruction Set Architecture (ISA) provided the ideal foundation for this approach [12, 36]. Unlike proprietary ISAs, RISC-V allows for the addition of custom instructions and, more importantly, the seamless integration of specialized hardware blocks. This flexibility is a cornerstone of the burgeoning ecosystem of open-source system-on-chip (SoC) design frameworks, such as Chipyard [39] and Rocket Chip [12], which were instrumental in the creation of our embedded platform. These frameworks provide a robust and configurable environment for building a processor core and integrating peripheral accelerators, enabling a highly tailored architecture that is optimized for our specific application domain [15, 37].

The single most resource-demanding operation in convolutional neural networks (CNNs) is the repeated multiplication of large matrices—specifically, the convolution operation itself, which involves multiplying an input feature map with a set of filter weights. General-purpose processors, even highly parallel ones, are not architecturally optimized for this type of dense, repetitive calculation. They are typically bottlenecked by memory bandwidth and the serial execution of instructions. This led us to develop a Tightly Coupled Accelerator (TCA) specifically for accelerating the convolutional and fully connected layers

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of the ChessNet model. The TCA is an on-chip block that operates in close proximity to the RISC-V core, sharing data paths and control signals for minimal communication overhead.

The core of our TCA is a systolic array, a highly efficient parallel architecture for matrix multiplication [34]. The array consists of a grid of simple processing elements (PEs), each of which can perform a multiply-accumulate operation. Data flows through the array in a rhythmic, "systolic" manner, with input activations and weights streamed into the array from different directions. This design ensures that each PE is continuously busy with computation, minimizing idle time and maximizing throughput. The parallelism of the systolic array directly maps to the parallelism inherent in a convolution, allowing us to compute a full output feature map in a fraction of the time required by a standard processor. This architecture is a well-established and highly effective technique for deep learning acceleration, as demonstrated in seminal works on efficient neural network processing [4, 15, 38].

A critical component of the TCA's efficiency is its dedicated, on-chip scratchpad memory. In a conventional system, data for computation (input feature maps, weights) must be fetched from the main dynamic random-access memory (DRAM), a process that is both slow and energy-intensive [14]. The scratchpad memory allows the RISC-V core to "stage" the necessary data for a convolutional layer directly onto the accelerator. Once the data is in the scratchpad, the TCA can perform the entire computation without further access to the main memory, thereby drastically reducing memory bandwidth requirements and associated energy consumption. This memory hierarchy, with a small, fast on-chip memory for the accelerator, is a hallmark of modern hardware-software co-design for deep learning [15, 37, 38].

On the software side, the challenge was to intelligently partition the ChessNet model for optimal execution on this heterogeneous architecture. The TensorFlow Lite framework, or a similar custom solution, was used to parse the trained model graph. A key software component, the graph optimizer, identifies the sequences of operations that are best suited for the TCA—primarily the convolution and matrix multiplication layers. The rest of the model, including non-linear activation functions (e.g., ReLU), pooling layers, and batch normalization, are computationally less demanding and are executed efficiently on the RISC-V general-purpose core [21]. This hardware-software interface is managed by a small runtime library that handles the data transfer to the scratchpad and orchestrates the execution on the TCA, treating it as a specialized co-processor [15].

The performance gains of this co-design approach are substantial and were the primary factor in achieving real-time performance. To quantify these gains, we conducted a detailed micro-architectural analysis of the ChessNet model's execution. A single convolutional layer in our model, when executed on the RISC-V core without the accelerator, took an average of 150 milliseconds. This high latency is a direct result of the core's inability to exploit the inherent data parallelism of the operation. By contrast, when the same layer was executed on the TCA, the average latency dropped to a mere 7.5 milliseconds. This represents an approximately 20x speedup for the most critical component of our system. When considering the energy consumption, the difference is even more dramatic. The TCA, with its specialized design and

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minimal memory traffic, consumed less than 50 milliwatts on average during inference, whereas the general-purpose core executing the same operation would draw over 500 milliwatts. This equates to more than an 80% reduction in energy consumption for the key computational task.

The impact of this acceleration on the overall system performance is profound. Without the TCA, the total system latency for a single frame, including image acquisition, localization, and inference, would be well over 300 milliseconds, making the system unsuitable for a real-time application. With the TCA, the inference time is reduced to the point where it is no longer the bottleneck. The total system latency of 150 milliseconds is now dominated by the classical computer vision algorithms for board localization and the data transfer overhead. This performance profile proves that even complex, real-world AI applications can be successfully deployed on low-cost hardware, provided that a full-stack, hardware-software co-design approach is employed from the outset [37].

This rigorous analysis confirms that the synergy between a flexible, open-source processor architecture like RISC-V and a custom-designed hardware accelerator is not merely a theoretical exercise but a practical and essential strategy for enabling the next generation of affordable and efficient intelligent edge devices. Our research provides a clear blueprint for engineers and researchers seeking to build similar systems for vision-based applications, proving that computational power need not be a barrier to entry when design is focused on optimizing for the specific task at hand.

3. RESULTS

3.1 Performance Evaluation

The system's performance was evaluated based on three key metrics: chessboard localization accuracy, piece recognition accuracy, and total system latency.

- Chessboard Localization Accuracy: The localization module achieved an accuracy of 99.5% on a test set of over 500 images captured under varying lighting conditions and from slightly different camera angles. The robust combination of Canny edge detection and the Hough transform proved highly resilient to minor distortions.

- Piece Recognition Accuracy: The ChessNet model demonstrated a piece recognition accuracy of 98.2% on a dedicated test set of 10,000 square images. This included both real and synthetic images. The model's low parameter count (approximately 0.5 MB) and optimized architecture allowed it to perform inference with extremely low latency.

- Total System Latency: The system achieved an average processing time of 150 milliseconds per frame, corresponding to a frame rate of approximately 6.7 frames per second. This speed is sufficient for real-time digitization and is well within the requirements for most chess-related applications, such as live

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game streaming or educational tools. This low latency is directly attributable to the hardware-software co-design approach and the use of the RISC-V hardware accelerator for CNN inference.

3.2 Benchmarking and Comparison

A direct comparison of our system with existing solutions highlights its key advantages. While high-end systems running on dedicated GPUs can achieve higher frame rates [17], their cost and power consumption are orders of magnitude greater. For instance, a typical GPU-based system might draw over 100 watts of power and cost thousands of dollars, whereas our prototype operates on less than 5 watts and the total bill of materials for the hardware is under $100. This makes our solution highly accessible for hobbyists, educational institutions, and emerging markets. The trade-off is a slightly lower maximum accuracy compared to models with billions of parameters, but the 98.2% accuracy is more than sufficient for practical use [10]. Systems based on more traditional computer vision techniques, such as scale-invariant feature transform (SIFT) [26] or oriented chamfer matching [27], often struggle with real-time performance and robustness to visual noise and variations in piece appearance. Our deep learning approach, despite its small size, offers superior generalization.

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4. DISCUSSION

The results demonstrate the successful implementation of a real-time, vision-based chessboard digitization system on a low-cost embedded platform. The system's ability to accurately and quickly localize the board and classify the pieces validates the core hypothesis that computationally intensive deep learning tasks can be effectively ported to resource-constrained hardware through a combination of algorithmic efficiency and hardware acceleration. The use of a custom, lightweight CNN architecture (ChessNet) was pivotal in achieving the required performance within the hardware's memory and processing limits. The decision to use a RISC-V-based platform also proved to be a powerful enabler, providing the necessary flexibility for custom hardware accelerators to offload the most demanding computational tasks [37].

The implications of this work are far-reaching. By providing an affordable and accessible solution, we open the door to a wide array of new applications. For example, the system could be integrated into a smart chessboard for live game broadcasting without the need for manual setup or sensors. It could also serve as the visual core for an educational tool that provides real-time feedback and analysis to players as they practice. Furthermore, the methodology presented here, which emphasizes algorithmic optimization and hardware-software co-design, can be generalized to other low-cost, real-time vision applications, such as object tracking or industrial inspection on the edge.

Despite its success, the system has certain limitations. While robust to typical variations, its performance may degrade under extreme and unusual conditions, such as very poor lighting, highly reflective board surfaces, or non-standard chess sets that deviate significantly from the training data. The reliance on a top-down camera view is also a constraint, as a side-angle or more dynamic viewpoint would require more complex pose estimation and 3D modeling. These are avenues for future research.

CONCLUSION

In conclusion, this paper presents a complete, practical, and affordable solution for a long-standing computer vision problem. We have shown that by carefully selecting and optimizing both the software algorithms and the underlying hardware platform, it is possible to bring the power of deep learning to the edge, enabling real-time intelligent systems that were previously confined to high-end, expensive hardware.

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